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EXAMINER	
MENDEZ, ZULMARIAM	
ART UNIT	**PAPER NUMBER**
1795	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/822,424	BASOL ET AL.	
	Examiner	Art Unit	
	Zulmariam Mendez	1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,13,14,16-18 and 23-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,13,14,16-18 and 23-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/14/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. In the Information Disclosure Statement (IDS) of August 14, 2007, submitted by the applicant, the examiner has considered the cited US Applications but they have been lined through as they are not printed publications available to the public, and as such will not be printed on the face of the patent if one is to be issue.

Claim Objections

2. Claim 4 is objected to because of the following informalities: line 4 of the instant claim reads "a **third fourth** including a side adjacent to the third elongated contact electrode", which should read "a **fourth isolator** including a side adjacent to the third elongated contact electrode". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-7, 13, 14, 16-18, 23-25, 27, 28, and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams et al. (US Patent no. 6,143,155).

With regard to claim 1, Adams discloses an apparatus for the simultaneous electrochemical metal plating and planarization of wafers (col. 1, lines 9-11) comprising: an electrode assembly configured to be immersed in a solution and configured to be positioned proximate to a conductive layer on a wafer in contact with said solution, the electrode assembly configured to have a longitudinal dimension extending to at least a periphery of a wafer (col. 4, lines 3-13), the electrode assembly including: a first elongated contact electrode/anode (510, see figure 7); a first isolator (550) including a side adjacent to the first elongated contact electrode/anode (510); a first elongated process electrode/cathode (570) including a side adjacent to an opposite side of the isolator (550) as shown in figure 7, the first isolator (550) protruding above top surfaces of the first elongated contact electrode/anode (510) and the first elongated process electrode/cathode (570); the electrodes (510 and 570) and the isolator are fastened together by a fastener/brush (595); and a voltage supply (660, see figure 5) configured to apply a potential difference between the contact electrodes and the process electrodes (col. 8, lines 41-44) to plate or electro-polish the conductive layer of the wafer, wherein the isolators are configured to prevent the contact electrodes and the process electrodes from physically contacting said wafer (col. 8, lines 11-13). Adams further discloses adding steps to the process through the use of multiple electrodes within the electrode assembly with the anode and cathode alternating, so that the process may be accomplished in a single pass of the assembly (col. 11, lines 39-49).

When adding additional electrode pairs to the apparatus of Adams, one of ordinary skill in the art would have been motivated to add an additional isolator between

the two pairs to prevent any adjacent electrodes from shorting. An additional advantage of additional electrode pairs would be to increase overall plating rate because the additional electrodes would also perform electroplating and would increase the amount of current capable of being applied to the work-piece.

With regard to claim 3, the isolators of Adams each include a plurality of passages (540 and 560) configured to allow a solution to flow through the electrode assembly as shown in figure 7.

With regard to claim 4, the electrochemical apparatus of Adams further discloses adding steps to the process through the use of multiple electrodes within the electrode assembly with the anode and cathode alternating, so that the process may be accomplished in a single pass of the assembly (col. 11, lines 39-49).

With regard to claims 5 and 6, the electrochemical apparatus of Adams further comprising a mechanism configured to produce relative motion between the electrode assembly and a conductive layer on a wafer which provides electro-polishing of wherein motion of said wafer across the elongated process electrodes is configured to electro-polish substantially an entire surface of said conductive layer (col. 4, lines 13-20 and col. 12, lines 1-11).

With regard to claim 7, Adams further discloses wherein the mechanism is configured to produce rotational motion between the electrode assembly and a conductive layer on wafer (col. 11, line 67 and col. 12, lines 1-11).

With regard to claim 13, Adams discloses an apparatus for the simultaneous electrochemical metal plating and planarization of wafers (col. 1, lines 9-11) comprising:

an electrode assembly configured to be immersed in a solution and configured to be positioned proximate to a conductive layer on a wafer in contact with said solution, the electrode assembly configured to have a longitudinal dimension extending to at least a periphery of a wafer (col. 4, lines 3-13), the electrode assembly including: a first elongated contact electrode/anode (510, see figure 7); a first isolator (550) including a side adjacent to the first elongated contact electrode/anode (510); a first elongated process electrode/cathode (570) including a side adjacent to an opposite side of the isolator (550) as shown in figure 7, the first isolator (550) protruding above top surfaces of the first elongated contact electrode/anode (510) and the first elongated process electrode/cathode (570); a compressible strips/brush (595) is disposed above the each of the insulation members (590 and 530) and between each of the elongated contact electrodes and the elongated process electrodes, top surfaces of the compressible strips being substantially coplanar (see figure 7); and a voltage supply (660, see figure 5) configured to apply a potential difference between the contact electrodes and the process electrodes (col. 8, lines 41-44) to plate or electro-polish the conductive layer of the wafer, wherein the isolators are configured to prevent the contact electrodes and the process electrodes from physically contacting said wafer (col. 8, lines 11-13). Adams further discloses adding steps to the process through the use of multiple electrodes within the electrode assembly with the anode and cathode alternating, so that the process may be accomplished in a single pass of the assembly (col. 11, lines 39-49). With regard to claim 14, Adams further discloses wherein the elongated contact electrodes/anodes (510) and the elongated process electrodes/cathodes (570) are

configured to electro-polish the conductive layer on the wafer without physical contact with the wafer (col. 8, lines 11-22).

With regard to claim 16, the electrochemical apparatus of Adams further comprising a mechanism configured to produce relative motion between the electrode assembly and a conductive layer on a wafer which provides electro-polishing of wherein motion of said wafer across the elongated process electrodes is configured to electro-polish substantially an entire surface of said conductive layer (col. 4, lines 13-20 and col. 12, lines 1-11).

With regard to claim 17, Adams further discloses wherein the mechanism is configured to produce rotational motion between the electrode assembly and a conductive layer on wafer (col. 11, line 67 and col. 12, lines 1-11).

With regard to claims 18 and 32, the electrode assembly of Adams includes: a first elongated contact electrode/anode (510, see figure 7); a first isolator (550); a first elongated process electrode/cathode (570); a compressible strips/brush (595) disposed above the each of the insulation members (590 and 530) and between each of the elongated contact electrodes (510) and the elongated process electrodes (570); and a voltage supply (660, see figure 5) configured to apply a potential difference between the contact electrodes and the process electrodes (col. 8, lines 41-44) to plate or electro-polish the conductive layer of the wafer. However, Adams doesn't explicitly disclose having different zones with multiple electrodes and isolators applying different potentials to electro-polish a conductive layer on a wafer at different rates.

Adams further discloses adding steps to the process through the use of multiple electrodes within the electrode assembly with the anode and cathode alternating, so that the process may be accomplished in a single pass of the assembly (col. 11, lines 39-49). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to have made a plurality of zones of electrodes and insulators in order to electroplate or electro-polish predetermined areas of the conductive surface at different rates.

With regard to claim 23, Adams teaches a fastener/brush (595) to maintain the electrode assembly fastened together but fails to teach wherein the fastener comprises a pin extending through transverse holes in the elongated contact electrodes, the isolators, and the elongated process electrodes. However, it is well known in the art that compression fitting the various parallel electrodes onto a bolt would have provided a stable, solid support for the electrodes to keep them from moving with respect to each other. Therefore, one having ordinary skill in the art at the time of the invention would have been motivated to provide bolts to the fastener (55) of Adams in order to add additional support to the electrode assembly and keep the electrodes from moving with respect to each other.

With regard to claims 24 and 25, Adams discloses having an insulator (550) separating contact electrodes/anodes (510) and process electrodes/cathodes (570) (col. 7, lines 61-67). Adams further discloses adding steps to the process through the use of multiple electrodes within the electrode assembly with the anode and cathode

alternating, so that the process may be accomplished in a single pass of the assembly (col. 11, lines 39-49).

With regard to claim 27, the insulation members (530, 550 and 590) and the compressible strips (595) of Adams each include a plurality of openings (520, 540, 545, 560, 565 and 580) extending through the insulation members and the compressible strips see figure 7, the openings configured to allow a solution to flow through the electrode assembly (col. 10, lines 30-48).

With regard to claim 28, the elongated contact electrodes/anodes (510) and the elongated process electrodes/cathodes (570) of Adams each include a plurality of grooves (520 and 580, see figure 7) extending through the elongated contact electrodes (510) and the elongated process electrodes (570), the grooves configured to allow a solution to flow through the electrode assembly (col. 10, lines 30-48).

With regard to claim 31, Adams discloses all of the structure as applied above to claim 13, wherein the elongate contact electrodes, the insulation members, and the elongate process each have an axis of elongation and a width transverse to the axis of elongation and parallel to a plane defined by the axes of elongation, but fails to teach wherein the widths are between about 1 and 10 mm. However Adams further discloses that the electrodes may be of a different size, shape or area to enhance or reduce the current densities under the electrodes and thereby adjust the relative plating and planarizing rate (col. 10, lines 22-25). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the shape, size or area of the electrodes in order to enhance or reduce the current densities under the

electrodes and thereby adjust the relative plating and planarizing rate.

With regard to claim 33 the top surfaces of the compressible strips/brush (595) are configured to contact the conductive surface of the wafer (col. 10, lines 26-29).

5. Claims 26, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams et al., as applied to claim 13 above, in view of Schimion (US Patent no. 6,071,384).

With regard to claim 26, Adams discloses all of the structure, as applied above to claim 13, but fails to teach wherein the compressible strips each comprise a material having a closed pore structure configured to prevent solution from flowing through the insulation members and the compressible strips.

Schimion an arrangement for the electro-galvanic coating of wafers, which travel through an electrolyte, enriched with a metal (col. 1, lines 8-10) comprising insulating strips (6a, 6b, see figure 4) protruding above the surface of the electrodes wherein the electrolyte is guided parallel with or against the strip travel direction (col. 3, lines 32-39). Even though Schimion doesn't explicitly disclose having the strips comprising a closed pore material, it is suggested by the fact that the solution is only flowing parallel with or against the strip travel direction.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to use the insulating strips of Schimion, in the electrochemical apparatus of Adams in order to flow the electrolyte solution only in only one direction against the conductive surface of the wafer.

With regard to claims 29 and 30, Adams discloses all of the structure as applied above to claim 13, wherein the insulators protrudes above the top surfaces of the elongate contact electrodes/anodes (510) and the elongate process electrodes/cathodes (570) wherein the isolators are configured to prevent the contact electrodes and the process electrodes from physically contacting said wafer (col. 8, lines 11-13), but fails to teach that the protrusion extends between about 1 and 10 mm, specifically between 2-5mm. However, Schimion discloses an arrangement for the electro-galvanic coating of wafers, which travel through an electrolyte, enriched with a metal (col. 1, lines 8-10) having insulating strips (6a, 6b), which protrude only by a few millimeters into the electrolyte in order to prevent a contact with the wafer/strip (2, see figure 4) (col. 5, lines 19-21). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to protrude the isolators by only a few millimeters, as taught by Schimion, in the electrochemical apparatus of Adams in order to prevent the electrodes from physically contacting the conductive surface of the wafer.

6. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Adams as applied to claim 33 above, and further in view of Palmgren et al. (US Patent no. 7,247,577).

With regard to claim 34, Adams teaches all of the structures, as applied to claim 33 above, but fails to teach that the pad (595) is abrasive.

However, Palmgren discloses a polishing process, particularly the planarization process used in the manufacturing of semiconductor devices (col. 1, lines 13-15)

comprising an abrasive polishing pad to planarize the conductive surface of a substrate and an electrical insulator that insulates the abrasive surface of a conditioning tool, which conditions the polishing pad (col. 2, lines 23) in order to extend the useful life of the abrasive surface of the conditioning tool by reducing the level of electrochemically driven corrosion (col. 2, lines 23-26). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to use insulating abrasive polishing pads as taught by Palmgren, in the electrochemical apparatus of Adams, in order to planarize the conductive surface of a work-piece extending the useful life of the abrasive surface of the conditioning tool by reducing the level of electrochemically driven corrosion.

Response to Arguments

Claim Rejections - 35 USC § 112

7. The rejection made to claim 18 has been withdrawn in view of Applicant's clarifying amendments.

8. Applicant's arguments, see page 13, with respect to the rejection of claim 1 under 35 U.S.C 102 (b) as being anticipated by Ichinose have been considered but are moot in view of the new grounds of rejection necessitated by the amendment.

9. Applicant's arguments, see page 14, with respect to the rejection of claim 13 under 35 U.S.C 1023(a) as being unpatentable over Ichinose in view of Wang have been considered but are moot in view of the new grounds of rejection necessitated by the amendment.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zulmariam Mendez whose telephone number is 571-272-9805. The examiner can normally be reached on Monday-Thursday, 8:30am-5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexa Neckel can be reached on 571-272-1446. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ZM 3/11

ALEXA D. NECKEL
SUPERVISORY PATENT EXAMINER